



P-Channel 8 V (D-S) MOSFET

PRODUCT SUMMARY							
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A) ^a	Q _g (Typ.)				
- 8	0.068 at V _{GS} = - 4.5 V	- 3.1					
	0.088 at V _{GS} = - 2.5 V	- 2.7	6.7 nC				
	0.155 at V _{GS} = - 1.5 V	- 2.1	0.7 110				
	0.290 at V _{GS} = - 1.2 V	- 0.5					

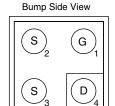
FEATURES

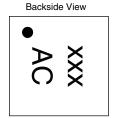
- TrenchFET® Power MOSFET
- Ultra Small 0.8 mm x 0.8 mm Outline
- Ultra Thin 0.357 mm Height
- Typical ESD Protection 1500 V HBM
- Material categorization: For definitions of compliance please see www.vishav.com/doc?99912



HALOGEN FREE

MICRO FOOT



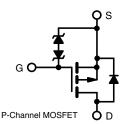


Device Marking: xxx = Date/Lot Traceability Code

Ordering Information: Si8805EDB-T2-E1 (Lead (Pb)-free and Halogen-free)

APPLICATIONS

- Portable Devices such as Cell Phones, Smart Phones, Tablet PCs and Media Players
 - Load Switch for Low Voltage Gate Drive
 - Load Switch for 1.2 V Power Line



Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V_{DS}	- 8	V	
Gate-Source Voltage		V_{GS}	± 5	v	
	T _A = 25 °C		- 3.1 ^a		
Continuous Drain Current (T = 150 °C)	T _A = 70 °C		- 2.5 ^a		
Continuous Drain Current (T _J = 150 °C)	T _A = 25 °C	- I _D	- 2.2 ^b		
	T _A = 70 °C		- 1.8 ^b	A	
Pulsed Drain Current		I _{DM}	- 15		
0 " 0 0 0 0	T _A = 25 °C		- 0.7 ^a		
Continuous Source-Drain Diode Current	T _A = 25 °C	I _S	- 0.4 ^b		
	T _A = 25 °C		0.9 ^a		
Mariana Barra Biasinatian	T _A = 70 °C		0.6 ^a	w	
Maximum Power Dissipation	T _A = 25 °C	- P _D	0.5 ^b	VV	
	T _A = 70 °C	1	0.3 ^b		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150	°C	
Soldering Recommendations (Peak Temperature) ^c			260		

THERMAL RESISTANCE RATINGS							
Parameter	Symbol	Typical	Maximum	Unit			
Maximum Junction-to-Ambient ^{a, d}	t≤5s	D	105	135	°C/W		
Maximum Junction-to-Ambient ^{b, e}	1238	R _{thJA}	200	260	C/VV		

Notes:

- a. Surface mounted on 1" x 1" FR4 board with full copper, $t=5\ s.$ b. Surface mounted on 1" x 1" FR4 board with minimum copper, $t=5\ s.$
- c. Refer to IPC/JEDEC (J-STD-020), no manual or hand soldering.
- d. Maximum under steady state conditions is 185 °C/W.
- e. Maximum under steady state conditions is 330 °C/W.

Si8805EDB

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SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)								
Parameter	Symbol	Min.	Тур.	Max.	Unit			
Static								
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$				V		
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I _D = - 250 μA		- 4	m)//°C			
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	1D = - 250 μΑ		2.1		mV/°C		
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = -250 \mu A$	- 0.35		- 0.7	V		
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 5 \text{ V}$			± 1.5			
Zara Cata Valtaga Drain Current	1	V _{DS} = -8 V, V _{GS} = 0 V			- 1	μΑ		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -8 V, V _{GS} = 0 V, T _J = 55 °C			- 10			
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \le -4 \text{ V}, V_{GS} = -4.5 \text{ V}$	- 5			Α		
		V _{GS} = - 4.5 V, I _D = - 1.5 A		0.056	0.068	Ω		
	В	V _{GS} = - 2.5 V, I _D = - 1.5 A		0.070	0.088			
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 1.5 V, I _D = - 0.5 A		0.115	0.155			
		V _{GS} = - 1.2 V, I _D = - 0.3 A		0.190	0.290			
Forward Transconductance ^a	9 _{fs}	V _{DS} = - 4 V, I _D = - 1.5 A		8		S		
Dynamic ^b								
Total Gate Charge	Qg			6.7	10	nC		
Gate-Source Charge	Q_{gs}	$V_{DS} = -4 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -1.5 \text{ A}$		0.7				
Gate-Drain Charge	Q_{gd}			1.8				
Gate Resistance	R_{g}	f = 1 MHz		10		Ω		
Turn-On Delay Time	t _{d(on)}			13	25			
Rise Time	t _r	$V_{DD} = -4 \text{ V}, R_{L} = 2.7 \Omega$		13	25	ns		
Turn-Off Delay Time	t _{d(off)}	$I_D \cong -1.5 \text{ A}, V_{GEN} = -4.5 \text{ V}, R_g = 1 \Omega$		25	50			
Fall Time	t _f			17	35			
Drain-Source Body Diode Characteristic	s							
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			- 0.7	Α		
Pulse Diode Forward Current	I _{SM}				- 15	^		
Body Diode Voltage	V_{SD}	I _S = - 1.5 A, V _{GS} = 0 V		- 0.8	- 1.2	V		
Body Diode Reverse Recovery Time	t _{rr}			35	70	ns		
Body Diode Reverse Recovery Charge	Q _{rr}	I _F = - 1.5 A,		15	30	nC		
Reverse Recovery Fall Time	t _a	dI/dt = 100 A/μs, T _J = 25 °C		15		ns		
Reverse Recovery Rise Time	t _b			20				

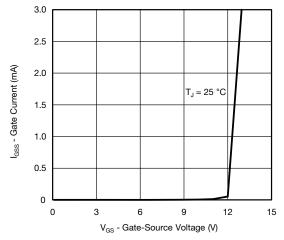
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %

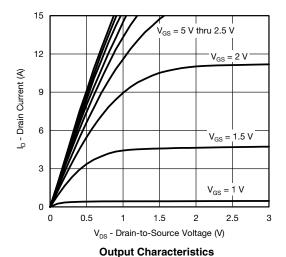
b. Guaranteed by design, not subject to production testing.

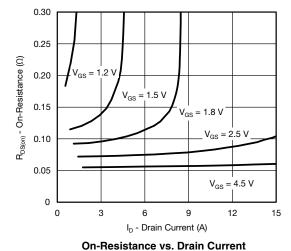


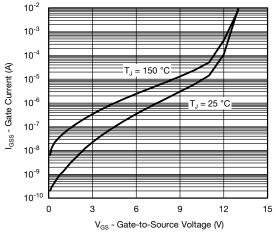
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



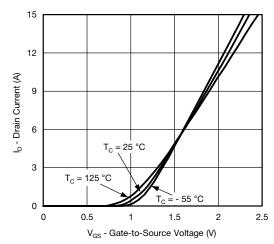
Gate Current vs. Gate-Source Voltage



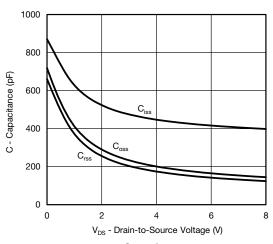




Gate Current vs. Gate-Source Voltage



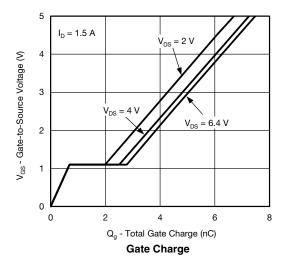
Transfer Characteristics

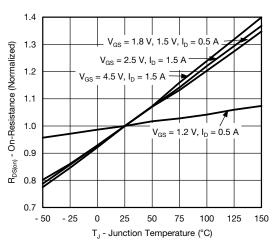


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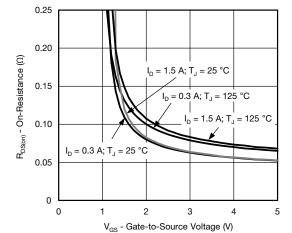
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

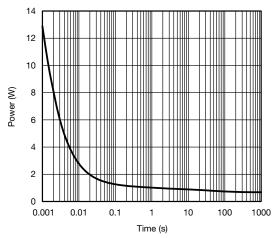




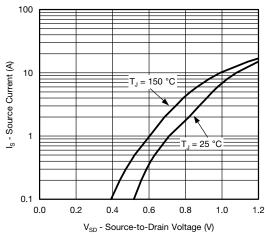
On-Resistance vs. Junction Temperature



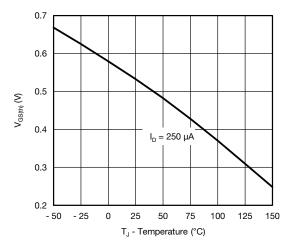
On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power (Junction-to-Ambient)



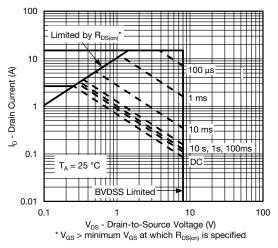
Source-Drain Diode Forward Voltage



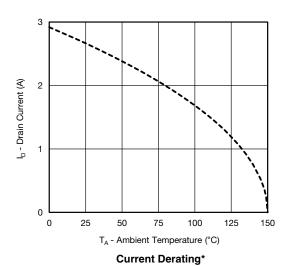
Threshold Voltage

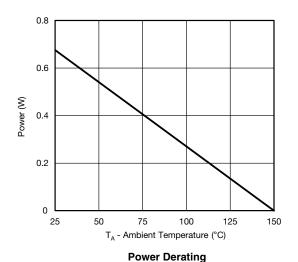


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Safe Operating Area, Junction-to-Ambient





Note:

When mounted on 1" x 1" FR4 with full copper.

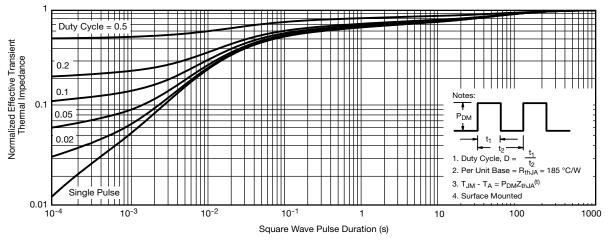
^{*} The power dissipation PD is based on TJ(max) = 150 °C, using junction-to-ambient thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heafsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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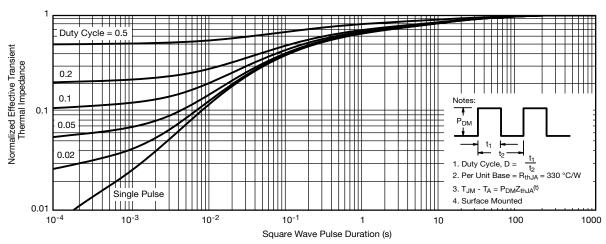
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient (on 1" x 1" FR4 board with maximum copper)

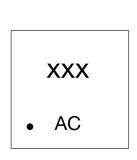


Normalized Thermal Transient Impedance, Junction-to-Ambient (on 1" x 1" FR4 board with minimum copper)

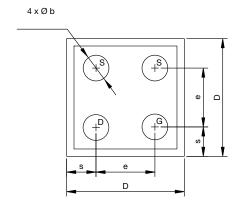


PACKAGE OUTLINE

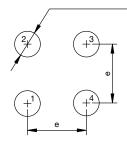
MICRO FOOT 0.8 mm x 0.8 mm: 4-BUMP (2 x 2, 0.4 mm PITCH)



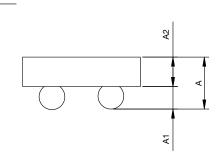
Mark on Backside of die



4 x Ø 0.205 to 0.225 Note 4 Solder Mask ~ Ø 0.215







Notes (unless otherwise specified):

- 1. All dimensions are in millimeters.
- 2. Four (4) solder bumps are lead (Pb)-free 95.5Sn/3.5Ag/0.7Cu with diameter Ø 0.165 mm to Ø 0.185 mm.
- 3. Backside surface is coated with a Ti/Ni/Ag layer.
- 4. Non-solder mask defined copper landing pad.
- 5. is location of pin 1.

Dim.	Millimeters ^a			Inches			
	Min.	Nom.	Max.	Min.	Nom.	Max.	
Α	0.314	0.357	0.400	0.0124	0.0141	0.0157	
A ₁	0.127	0.157	0.187	0.0050	0.0062	0.0074	
A ₂	0.187	0.200	0.213	0.0074	0.0079	0.0084	
b	0.165	0.175	0.185	0.0064	0.0068	0.0072	
е	0.400			0.0157			
s	0.180	0.200	0.220	0.0070	0.0078	0.0086	
D	0.760	0.800	0.840	0.0299	0.0314	0.0330	

a. Use millimeters as the primary measurement.

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